

09/08/2020

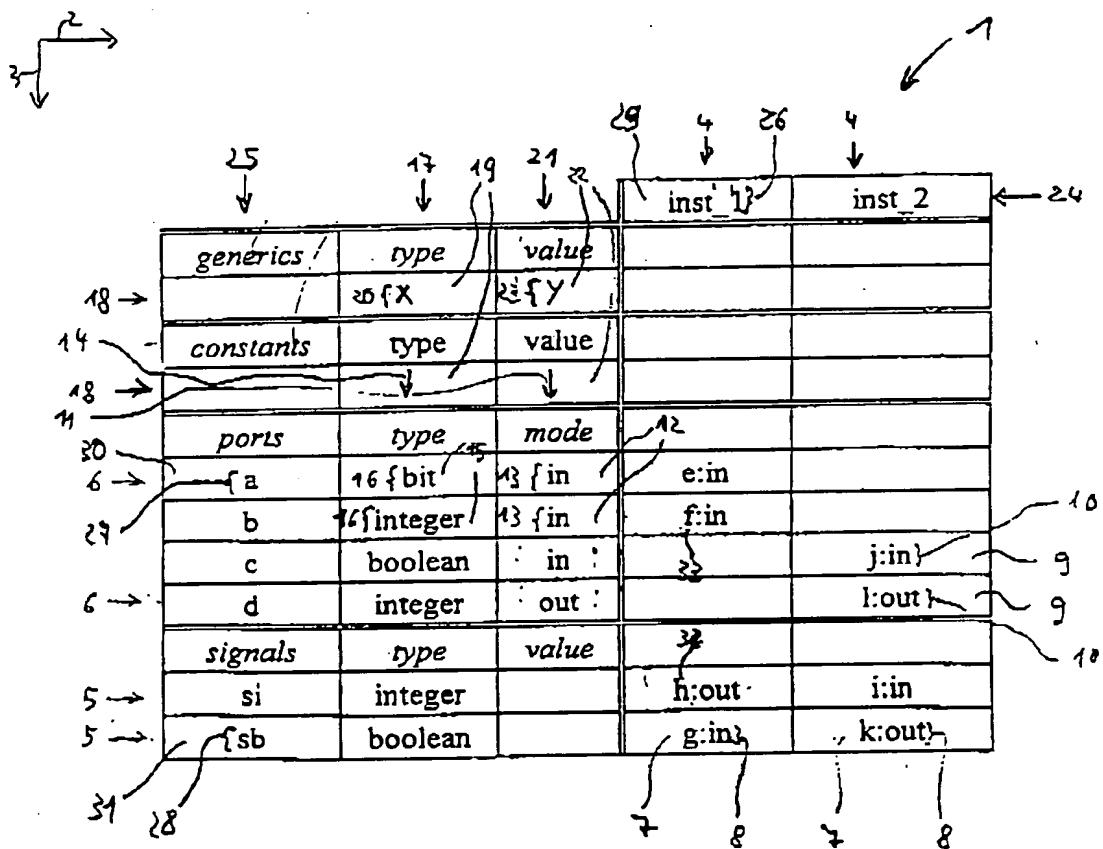


Fig. 1

1

identifier	mode	type	value	inst_1	inst_2	p0	p0
y	in	integer	3				
ci	in	integer	22	23			
---	---	integer	4	x <sub>40</sub>			
a	in	bit	15				
b	in	integer	36	1, in, , 7	42		
c	in	boolean	true				
d	out	integer		1, out			
si_1		integer				10	si_1, in
si_2		integer					si_1 + ci <sub>43</sub>
sb		bit		g, in	k, out		

2

signals	constants	entities	ports(entity)	ports(entity)	ports(entity)	ports(entity)	ports(entity)
5	18	38	6	6	6	6	6
5	18	38	6	6	6	6	6
5	18	38	6	6	6	6	6
5	18	38	6	6	6	6	6

Fig. 2